

# USB4 1.0 ENGINEERING CHANGE NOTICE FORM

**Title:** Clarify HW Margin Results

**Applied to:** USB4 Specification Version 1.0

<b>Brief description of the functional changes:</b>
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Clarifies how the High/Right and Low/Left Margin results are reported for a HW margin test.
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<b>Benefits as a result of the changes:</b>
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Eliminates confusion and ensure consistency with how the HW margin results are reported.
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<b>An assessment of the impact to the existing revision and systems that currently conform to the USB specification:</b>
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<b>An analysis of the hardware implications:</b>
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<b>An analysis of the software implications:</b>
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<b>An analysis of the compliance testing implications:</b>
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## Actual Change

### (a). Section 8.3.2.3.2

Table 8-70. RUN\_HW\_LANE\_MARGINING Completion Data

DW	Bit(s)	Field Name and Description
0	2:0	<b>Lane Select</b> This field contains the value of the Lane Select field in the last RUN_HW_LANE_MARGINING Port Operation.
	3	<b>Timing Margin Test</b> This field contains the value of the Timing Margin Test field in the last RUN_HW_LANE_MARGINING Port Operation.
	4	<b>Enable Margin Tests</b> This field contains the value of the Enable Margin Tests field in the last RUN_HW_LANE_MARGINING Port Operation.
	9:5	<b>BER Level Contour</b> This field contains the value of the <i>BER Level Contour</i> field in the last RUN_HW_LANE_MARGINING Port Operation.
	10	<b>Enable Optional Voltage Offset Range</b> This field contains the value of the <i>Enable Optional Voltage Offset Range</i> field in the last RUN_HW_LANE_MARGINING Port Operation.
	31:11	<b>Reserved.</b>
1	6:0	<b>High / Right Margin (Lane 0)</b> <u>For a voltage margin test, this field contains the high margin test result for Lane 0 in terms of number of voltage offset steps to the BER Level Contour. If the high margin exceeds the Maximum Voltage Offset this field contains the maximum voltage offset step which was applied during the test. See Note 1.</u> <u>For a time margin test, this field contains the right margin test result for Lane 0 in terms of number of time offset steps to the BER Level Contour. If the right margin exceeds the Maximum Time Offset this field contains the maximum right offset step which was applied during the test. See Note 2.</u> <del>For a voltage margin test, this field contains the high margin test result for Lane 0 in units of ceiling(Maximum Voltage Offset / Voltage Margin Steps). If the high margin exceeds the Maximum Voltage Offset this field contains the maximum voltage offset which was applied during the test in units of ceiling(Maximum Voltage Offset / Voltage Margin Steps).</del> <del>For a time margin test, this field contains the right margin test result for Lane 0 in units of ceiling(Maximum Time Offset / Time Margin Steps). If the right margin exceeds the Maximum Time Offset this field contains the maximum right offset which was applied during the test in units of ceiling(Maximum Voltage Offset / Voltage Margin Steps).</del>
1	7	<b>High / Right Margin Exceeds Maximum Voltage / Time Offset (Lane 0)</b> For a voltage margin test, this field indicates if the high margin exceeds the Maximum Voltage Offset for Lane 0: 0b: High margin does not exceed the Maximum Voltage Offset 1b: High margin exceeds the Maximum Voltage Offset For a time margin test, this field indicates if the right margin exceeds the Maximum Time Offset for Lane 0: 0b: Right margin does not exceed the Maximum Time Offset 1b: Right margin exceeds the Maximum Time Offset

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DW	Bit(s)	Field Name and Description
	14:8	<p><b>Low / Left Margin (Lane 0)</b></p> <p><u>For a voltage margin test, this field contains the low margin test result for Lane 0 in terms of number of voltage offset steps to the BER Level Contour. If the Low margin exceeds the Maximum Voltage Offset this field contains the maximum voltage offset step which was applied during the test. See Note 3.</u></p> <p><u>For a time margin test, this field contains the left margin test result for Lane 0 in terms of number of time offset steps to the BER Level Contour. If the left margin exceeds the Maximum Time Offset this field contains the maximum left offset step which was applied during the test. See Note 4.</u></p> <p><u>For a voltage margin test, this field contains the low margin test result for Lane 0 in units of ceiling(Maximum Voltage Offset / Voltage Margin Steps). If the low margin exceeds the Maximum Voltage Offset this field contains the maximum voltage offset which was applied during the test in units of ceiling(Maximum Voltage Offset / Voltage Margin Steps).</u></p> <p><u>For a time margin test, this field contains the left margin test result for Lane 0 in units of ceiling(Maximum Time Offset / Time Margin Steps). If the left margin exceeds the Maximum Time Offset this field contains the maximum left offset which was applied during the test in units of ceiling(Maximum Voltage Offset / Voltage Margin Steps).</u></p>
	15	<p><b>Low / Left Margin Exceeds Maximum Voltage / Time Offset (Lane 0)</b></p> <p>For a voltage margin test, this field indicates if the low margin exceeds the Maximum Voltage Offset for Lane 0:</p> <p>0b: Low margin does not exceed the Maximum Voltage Offset 1b: Low margin exceeds the Maximum Voltage Offset</p> <p>For a time margin test, this field indicates if the left margin exceeds the Maximum Time Offset for Lane 0:</p> <p>0b: Left margin does not exceed the Maximum Time Offset 1b: Left margin exceeds the Maximum Time Offset</p>
	22:16	<p><b>High / Right Margin (Lane 1)</b></p> <p><u>For a voltage margin test, this field contains the high margin test result for Lane 1 in terms of number of voltage offset steps to the BER Level Contour. If the high margin exceeds the Maximum Voltage Offset this field contains the maximum voltage offset step which was applied during the test. See Note 1.</u></p> <p><u>For a time margin test, this field contains the right margin test result for Lane 1 in terms of number of time offset steps to the BER Level Contour. If the right margin exceeds the Maximum Time Offset this field contains the maximum right offset step which was applied during the test. See Note 2.</u></p> <p><u>For a voltage margin test, this field contains the high margin test result for Lane 1 in units of ceiling(Maximum Voltage Offset / Voltage Margin Steps). If the high margin exceeds the Maximum Voltage Offset this field contains the maximum voltage offset which was applied during the test in units of ceiling(Maximum Voltage Offset / Voltage Margin Steps).</u></p> <p><u>For a time margin test, this field contains the right margin test result for Lane 1 in units of ceiling(Maximum Time Offset / Time Margin Steps). If the right margin exceeds the Maximum Time Offset this field contains the maximum right offset which was applied during the test in units of ceiling(Maximum Voltage Offset / Voltage Margin Steps).</u></p>
	23	<p><b>High / Right Margin Exceeds Maximum Voltage / Time Offset (Lane 1)</b></p> <p>For a voltage margin test, this field indicates if the high margin exceeds the Maximum Voltage Offset for Lane 1:</p> <p>0b: High margin does not exceed the Maximum Voltage Offset 1b: High margin exceeds the Maximum Voltage Offset</p> <p>For a time margin test, this field indicates if the right margin exceeds the Maximum Time Offset for Lane 1:</p> <p>0b: Right margin does not exceed the Maximum Time Offset 1b: Right margin exceeds the Maximum Time Offset</p>

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DW	Bit(s)	Field Name and Description
	30:24	<p><b>Low / Left Margin (Lane 1)</b></p> <p><u>For a voltage margin test, this field contains the low margin test result for Lane 1 in terms of number of voltage offset steps to the BER Level Contour. If the low margin exceeds the Maximum Voltage Offset this field contains the maximum voltage offset step which was applied during the test. See Note 3.</u></p> <p><u>For a time margin test, this field contains the left margin test result for Lane 1 in terms of number of time offset steps to the BER Level Contour. If the left margin exceeds the Maximum Time Offset this field contains the maximum left offset step which was applied during the test. See Note 4.</u></p> <p><u>For a voltage margin test, this field contains the low margin test result for Lane 1 in units of ceiling(Maximum Voltage Offset / Voltage Margin Steps). If the low margin exceeds the Maximum Voltage Offset this field contains the maximum voltage offset which was applied during the test in units of ceiling(Maximum Voltage Offset / Voltage Margin Steps).</u></p> <p><u>For a time margin test, this field contains the left margin test result for Lane 1 in units of ceiling(Maximum Time Offset / Time Margin Steps). If the left margin exceeds the Maximum Time Offset this field contains the maximum left offset which was applied during the test in units of ceiling(Maximum Voltage Offset / Voltage Margin Steps).</u></p>
1	31	<p><b>Low / Left Margin Exceeds Maximum Voltage / Time Offset (Lane 1)</b></p> <p>For a voltage margin test, this field indicates if the low margin exceeds the Maximum Voltage Offset for Lane 1:</p> <p>0b: Low margin does not exceed the Maximum Voltage Offset</p> <p>1b: Low margin exceeds the Maximum Voltage Offset</p> <p>For a time margin test, this field indicates if the left margin exceeds the Maximum Time Offset for Lane 1:</p> <p>0b: Left margin does not exceed the Maximum Time Offset</p> <p>1b: Left margin exceeds the Maximum Time Offset</p>
<p><u>Note 1. The High Margin test result can be reported by application software in units of mV by the following conversion:</u></p> $\text{High Margin (mV)} = \text{High Margin (steps)} \times \text{Maximum Voltage Offset (mV)} \div \text{Voltage Margin Steps (steps)}$ <p><u>Note 2. The Right Margin test result can be reported by application software in units of UI by the following conversion:</u></p> $\text{Right Margin (UI)} = \text{Right Margin (steps)} \times \text{Maximum Time Offset (UI)} \div \text{Time Margin Steps (steps)}$ <p><u>Note 3. The Low Margin test result can be reported by application software in units of mV by the following conversion:</u></p> $\text{Low Margin (mV)} = \text{Low Margin (steps)} \times \text{Maximum Voltage Offset (mV)} \div \text{Voltage Margin Steps (steps)}$ <p><u>Note 4. The Left Margin test result can be reported by application software in units of UI by the following conversion:</u></p> $\text{Left Margin (UI)} = \text{Left Margin (steps)} \times \text{Maximum Time Offset (UI)} \div \text{Time Margin Steps (steps)}$		